International Journal of Electrical, Electronics and Computer Engineering **3**(1): 162-167(2014)

ISSN No. (Online): 2277-2626

Self Biased Complementary Differential Amplifier for Liquid Crystal Display

Shubhhangi Shrivastava and Rahul Mishra

Department of Electronic and Communication Engineering, LNCT, Bhopal, (MP), India

(Corresponding author Shubhhangi Shrivastava)

(Received 05 May, 2014 Accepted 04 June, 2014)

ABSTRACT: The proposed buffer achieves high-speed, draws a small quiescent current during static operation and offers a rail-to-rail in between input & output using complementary MOS differential amplifier. The circuit provides enhanced slew rate with a low power consumption by exploiting two current comparators embodied in the input stage, which sense the input signal transients to turn on the output stage transistors. A rail-to-rail stacked mirror differential amplifier is used to amplify the input signal difference and supply the bias voltages for the output stage. Simulations show that the proposed buffer can drive a 2-nF column line load within .6µs settling time under a full voltage swing, while drawing only 4µA static current, with slew rate 12v/µs, power consumption is 1.05 mW, for 3-V power supply.

I. INTRODUCTION

in the recent advancement liquid crystal display becomes one of the most popular display device many computers electronics graduates uses it as a display unit each pixel requires an output buffer for high quality display.

To drive having the resistance and capacitive load the widely used class AB buffer amplifier. A display unit consist of source driver, gate driver, timing controller, voltage transformer, reference voltage generator and Gamma correction voltage levels. The column driver of the LCD is the most important part in LCD architecture for Fast speed high resolution low power dissipation are controlled by column driver. An and LCD column driver generally includes digital to analog converter, data latch, shift registers and output buffers among these output buffers is the most dominant to define the speed, resolution, voltage swing and power consumption as the display pixel are always updated row-by-row, the output buffers must be driven by a step size function so there output voltage should be settled within the horizontal scanning time.

LCD output buffer are commonly realized by two stage operational amplifier in unity feedback configuration since to increase the phase margin use Miller compensation capacitor which involve high area consumption, so to avoid this at output node we use dominant pole to exploit them Miller capacitance, to provide high-speed driving capability we use current comparators at output in order to improve not only high-speed but also decreases power consumption during static and increases slew rate.

Lu *et al.* [1-9] proposed some class-AB output buffers for flat-panel-display application, for which the driving capabilities of the circuit are achieved by adding comparators which sense the rising and/or falling edges of the input waveform to turn on a push/pull transistor to charge/discharge the output load. Yu et al. [10] proposed a class-B output buffer for flat-panel-display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage. Kim *et al.* [11] proposed a multi-level multi-phase charge-recycling method for low-power AMLCD column drivers. The author proposed this charge-recycling method to reduce the power consumption incurred in driving highly capacitive column lines by storing the charge into the external capacitors and reusing it in the next cycle. Itakura *et al.* [8-15] proposed an output amplifier in which the phase compensation is achieved by introducing a zero, which is formed by the load capacitance and the phase compensation resistor connected between the output of the amplifier and the capacitive load.

II. PROPOSED BUFFER AMPLIFIER

Figure 1 block diagram of proposed buffer amplifier it is divided into two stage process stages RAIL TO RAIL complement CMOS differential amplifier A1 and second is stage consist of common source amplifier A2 and to current comparators C1 & C2 and an output push-pull amplifier consist of M01 & M02, second section is operated in class AB mode.

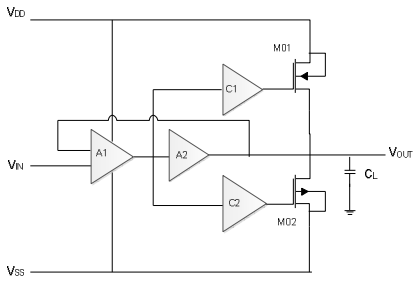

Fig.1. Block diagram of proposed.

The complimentary MOS differential amplifier is used to obtain RAIL-to-Rail in between input and output it actually takes advantage of both PMOS and NMOS differential amplifier, as we have seen there is miller capacitance is used as the dominant pole is located at output load due to this configuration the slew rate is not affected by first stage amplifier it is affected only by second stage output. As there is no compensation resistor used so output settling time depends upon the internal resistance of the output push-pull stage.

III. DESIGN ASPECTS AND OPERATING PRINCIPLE

The proposed buffer configuration contains biasing network (MB1-MB8), complementary MOS differential amplifier, PMOS differential amplifier M1 & M2 for biasing, M11,M12 for differential gain & M16,M20 for active load similarly for NMOS differential amplifier M3 & M4 for biasing, M9,M10 for differential gain & M13,M17 for active load, from M1-M22 all together constitute complementary differential amplifier working in class AB due to M21 & M22 as shown in fig 2.Both complementary pairs of the input differential amplifier are designed to draw the same current value $nI_{B1}/2$, whereI_{B1} is the quiescent current supplied by the bias network devices MB1-MB4 and n is the mirror factor of current sourcesM1 and M4, defined as

$$n = \frac{\left(\frac{W}{L}\right)_{MB1}}{\left(\frac{W}{L}\right)_{M1}} = \frac{\left(\frac{W}{L}\right)_{MB4}}{\left(\frac{W}{L}\right)_{M4}}$$

Assuming an equal aspect ratio for transistors M13-M16 and M17-M20, the currents in both branches of the folded-cascode mirror have the same value. Hence, the drain voltages of M14and M15 are respectively equal to those of M18 and M19. The currents flowing in M14 and M18 are given by

$$I_{M18} = I_{M17} = n\frac{I_{12}}{2} + I_{14}$$

WhereI_{B2} is the drain current of M14 and M18. Since the gate voltages of M21 and M22 are respectively sizing of the current mirror factors of the folded-cascode input stage, and no additional biasing networks are required to maintain an almost constant output current equal to those of M14 and M18, Therefore, the output quiescent current of the amplifier class-AB section can get opportunely set by means of an appropriate, Two current comparators M23, M24 and M25,M26 and a push-pull O/P stage M27&M28, the comparators are used to amplify the voltage difference of the two i/p's, according to the O/P's of the comparator turn ON/OFF the transistor of the O/P stage. On the other side, to ensure the other driving devices M27 and M28 to stay off during static operation to save in power consumption, the DC drain currents of M23 and M26 are designed to be slightly lower than the nominal drain currents of M24 and M25, respectively. The above specification is fulfilled upon the following design conditions

$$\frac{\left(\frac{W}{L}\right)_{M23}}{\left(\frac{W}{L}\right)_{13}} = \frac{\left(\frac{W}{L}\right)_{M24} - \Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)_{16}}$$

$$\frac{\left(\frac{W}{L}\right)_{M26}}{\left(\frac{W}{L}\right)_{16}} = \frac{\left(\frac{W}{L}\right)_{M25} - \Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)_{13}}$$

implying the gate voltages of M27 and M28 to quickly move towards the highest and lowest supply voltages, respectively, causing both auxiliary devices to be cut off from the output. when Vin(+) decreases the current in M10 & M12 will increase ,but the current in M9 & M11 will decrease, the gate voltage M17 & M16 will increase this will make M23 to be in triode region and that M24 in saturation region, so the drain voltage of M24 will increase and makes M28 to turn ON to discharge the O/P load & M27 is cutoff, until M26 is fully On to discharge. A table1.shows aspects ratio of MOS used in schema.

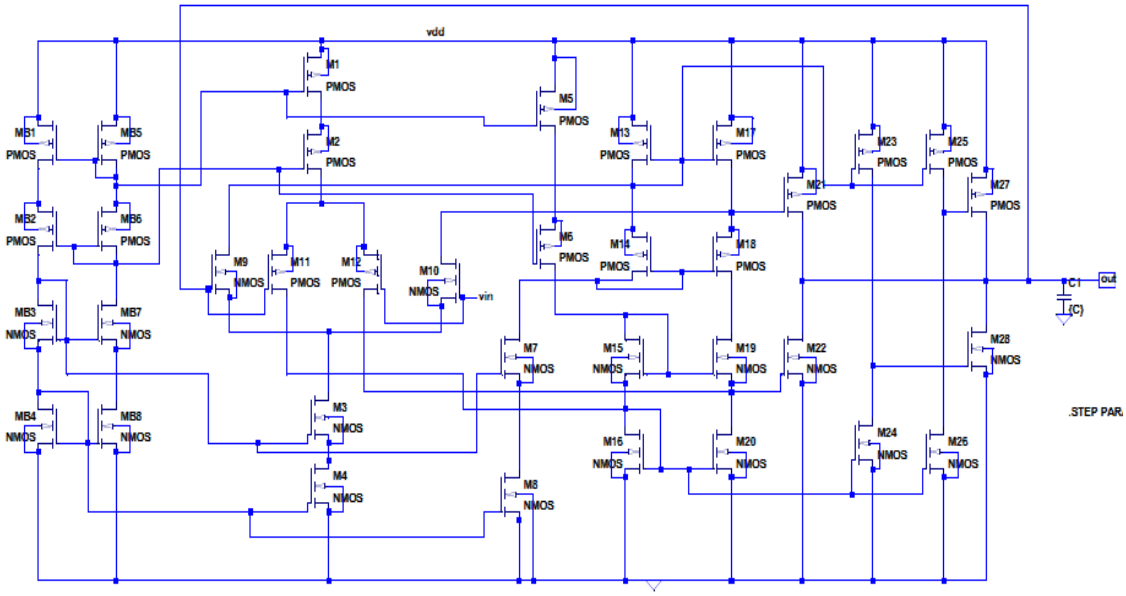

Fig. 2. Schematic of proposed buffer.

Table 1. Aspect ratio of MOS used in buffer.

Device	Dimension
MB1, MB4, MB5, MB8,M5,M8	5x(1/2.8)
MB2, MB3, MB6, MB7,M6,M7	1x(1/2.8)
M1,M2,M3,M4,M21,M22	10x(1/2.8)
M9,M10,M11,M12	20x(1.5/.6)
M13, M16, M17, M20	(1.2/0.7)
M14,M15, M18, M19	(0.6/0.7)
M22,M26	(0.6/0.6)
M24, M25	(1.8/0.6)
M27, M28	(20/1)

IV. SMALL-SIGNAL ANALYSIS

This section briefly analyzes the small-signal features of the proposed driving scheme. The simplified equivalent circuit of the proposed output buffer is depicted in Fig. 3, gm1 where and gm2 are the small-signal trans-conductance of the rail-to-rail stacked-mirror differential amplifier and the push-pull output gain stages, respectively, and R_{o1}, R_{o2}, and C_{o1}, C_{o2} are the equivalent output resistances and capacitances, respectively, of the relevant amplifier stages, whereas R_C is the compensation resistor and C_L is the equivalent capacitance of the LCD panel. In the present analysis, a simple capacitive-load model of the LCD panel is adopted because the worst-case stability condition is considered, since a distributed RC load would help the amplifier stability [22-28].

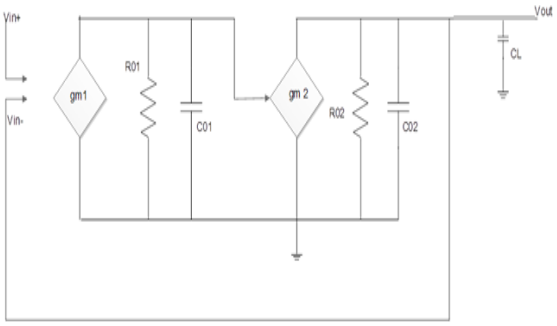

Fig. 3 Small signal analysis of the proposed buffer.

Assuming Ro1, Ro2 >> RC and Co1, Co2 << CL yields, in the most general case, the following

$$A_V(s) = A_o \frac{\left(1+\frac{s}{WZ}\right)}{\left(1+\frac{s}{WP1}\right)\left(1+\frac{s}{WP2}\right)\left(1+\frac{s}{WP3}\right)} \quad (1)$$

Where A_o is the DC open-loop gain expressed by

$$A_O = g_{m1} \cdot R_{o1} g_{m2} R_{o2} \quad (2)$$

while w_{P1},w_{P2} and w_{P3} are the frequencies of the three amplifier real poles, which are, respectively, given by

$$w_{P1} = \frac{1}{(Ro2 + Rc)C_L} \approx \frac{1}{Ro2C_L} \quad (3)$$

$$w_{P2} = \frac{1}{R_{o1}\, C_{o1}} \quad (4)$$

$$w_{P3} = 1/((Ro2 \parallel Rc)\, C_{\downarrow}o3\,) \approx 1/(R_1 C\ C_{\downarrow}o3\,) \quad (5)$$

and w_Z is the frequency of the left-half plane zero introduced by the compensation resistor R_C, which is given by

$$w_Z = \frac{1}{R_C[(C]_L + CO2)} \quad (6)$$

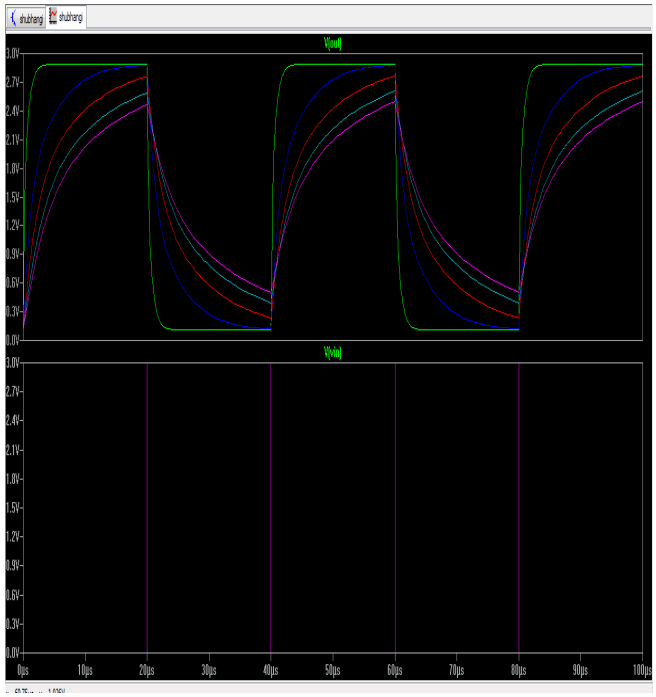

Fig. 4. Simulation result of proposed buffer with different capacitive load 100p-2000p with square wave.

The equivalent circuit contains three poles. However, the third pole frequency, w_{P3}, is far away from the other poles, and its contribution to the amplifier transfer function in (1) is negligible. The dominant pole of the circuit originates from the high-valued load capacitance, while the second pole frequency is determined by the equivalent resistance and capacitance of the amplifier internal node, and does not depend on the load capacitor. The compensation resistance and the load capacitance.

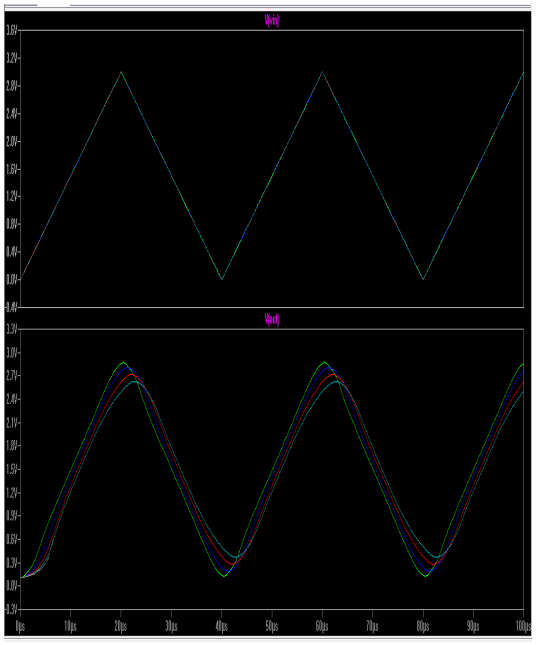

Fig. 5. Simulation result of proposed buffer with different capacitive load 100p-2000p with triangular wave.

CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB buffer amplifier is implemented prosperously. With different capacitive load from 100p to 2000p as shown in fig 4 & fig 5 with square and triangular wave. A comparison table 2 show the different parameters in comparison with previous results.

FUTURE SCOPE

Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilises a only 0.74 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas-

* Since power consumption is low, it has a great future in getting utilized in applications like "ultra low power ADCs".
* Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in "image exhibit contrivances, flat panel exhibits etc.
*Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks. Above are just few examples, but this buffer is having excellent usability in many other areas also.

REFERENCES

[1]. Chih-Wen Lu, "High-Speed Driving and Compact High- Speed Low-power Rail-to-Rail Class-B Buffer Amplifier for Small- and Large-size LCD Applications," accepted by *IEEE Journal of Solid-State Circuit.*

[2]. Ming-Chan Weng and Jiin-Chuan Wu, "A Compact Low- Power Rail-to-Rail Class-B Buffer for LCD Column Driver," *IEICE Trans. Electron.,* Vol. **E85-C**, No. 8 August, pp. 1659- 1663, 2002.

[3]. Pang-Cheng Yu and Jiin-Chuan Wu, "A Class-B Output Buffer for Flat-Panel-Display Column Driver," *IEEE Journal of Solid-State Circuits,* Vol. **34**, No.1, Jan. pp. 116-119, 1999.

[4]. D. J. R. Cristaldi, S. Pennisi, and F. Pulvirenti, Liquid Crystal Display Drivers: Techniques and Circuits. New York: Springer, Mar. 2009.

[5]. S. Di Fazio, S. Pennisi, F. Pulvirenti, and T. Signorelli, "670-nA CMOS OTA for AMLCD column driver," *J. Circuits, Syst., Comput.,* vol. **18**, no. 2, pp. 339–350, Apr. 2009.

[6]. R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits,* vol. **29**, no. 12, pp. 1505–1513, Dec. 1994.

[7]. T. Itakura, "A high slew-rate operational amplifier for an LCD driver IC," *IEICE Trans. Fundamentals*, vol. **E78-A,** no. 2, pp. 191–195, Feb. 1995.

[8]. T. Itakura and H. Minamizaki, "10- .A quiescent current opamp design for LCD driver ICs," *IEICE Trans. Fundamentals*, vol**. E81-A**, no. 2, Feb. 1998.

[9]. C.-W. Lu, "Low-power high-speed class-AB buffer amplifiers for liquid crystal display signal driver application," *J. Circuits, Syst., Computer.*, vol. **11**, no. 4, pp. 427–444, Aug. 2002.

[10]. C.-W. Lu and K. Hsu, "A high-speed low-power rail-to-rail column driver for AMLCD application," *IEEE J. Solid-State Circuits, vol.* **39**, no. 8, pp. 1313–1320, Aug. 2004.

[11]. Y. S. Son, J. H. Kim, H. H. Cho, J. P. Hong, J. H. Na, D. S. Kim, D. K. Han, J. C. Hong, Y. J. Jeon, and G. H. Cho, "A column driver with low-power area-efficient push-pull buffer amplifiers for active-matrix LCDs," ISSCC Dig. Tech. Papers, pp. 142–143, Feb. 2007.

[12]. R. Ito, T. Itakura, and H. Minamizaki, "A class-AB amplifier for LCD driver," in *IEEE Symp. on VLSI* Circuits, June 2007, pp. 148–149.

[13]. P.-C. Yu and J.-C. Wu, "A class-B output buffer for flat-panel-display column driver," *IEEE J. Solid-State Circuits,* vol. **34**, no. 1, pp. 116–119, Jan. 1999.

[14]. C.-W. Lu and C. L. Lee, "A low-power high-speed class-AB buffer amplifier for flat-panel-display application," *IEEE Trans. Very Large- Scale Integr.* (VLSI) Syst., vol. **10**, no. 4, pp. 163–168, Apr. 2002.

[15]. M.C. Weng and J.-C. Wu, "A compact low-power rail-to-rail class-B buffer for LCD column driver," *IEICE Trans. Electron.,* vol. **E85-C**, no. 8, pp. 1659–1663, Aug. 2002.

[16]. T. Itakura and H. Minamizaki, "A two-gain-stage amplifier without an on-chip miller capacitor in an LCD driver IC," *IEICE Trans. Fundamentals*, vol. **E85-A**, no. 8, pp. 1913–1920, Aug. 2002.

[17]. T. Itakura, H. Minamizaki, T. Satio, and T. Kuroda, "A 402-output TFT-LCD driver IC with power control based on the number of colors selected," *IEEE J. Solid-State Circuits*, vol. **38**, no. 3, pp. 503–510, Mar. 2003.

[18]. C.W. Lu, "High-speed driving scheme and compact high-speed low power rail-to-rail class-B buffer amplifier for LCD applications," *IEEE J. Solid-State Circuits*, vol. **39**, no. 11, pp. 1938–1947, Nov. 2004.

[19]. C.-W. Lu and P. H. Xiao, "A high-speed low-power rail-to-rail buffer amplifier for LCD application," in Proc. CCECE '06, Dec. 2006, pp. 709–712.

[20]. J.H. Wang, J.-C. Qiu, H.-Y. Zheng, C.-H. Tsai, C.-Y. Wang, C.-C. Lee, and C.-T. Chang, "A compact low-power high slew-rate rail-to rail class-AB buffer amplifier for LCD driver ICs," in Proc. EDSS '07, Dec. 2007, pp. 397–400.

[21]. D. Marano, G. Palumbo, and S. Pennisi, "Improved low-power high speed buffer amplifier with slew-rate enhancement for LCD applications," J. Circuits, Syst., Comput., to be published.

[22]. R. Mita, G. Palumbo, and S. Pennisi, "Low-voltage high-drive CMOS current feedback opamp," *IEEE Trans. Circuits Syst. II,* vol. **52**, pp. 317–321, June 2005.

[23]. M. Annese, S. Bertaiola, G. Croce, A. Milani, R. Roggero, P. Galbiati, and C. Costiero, "0.18 .. BCD-High Voltage Gate (HVG) process to address advanced display drivers roadmap," *Proc. Power Semiconductor Devices and ICs*, pp. 363–366, 2005.

[24]. Chih-Wen Lu and Kuo Jen Hsu, "A High-Speed Low-Power Rail-to-Rail Column Driver for AMLCD Application" *IEEE Journal of Solid-State Circuits,* vol. **39**, pp. 1313-1320, Aug., 2004.

[25]. Chih-Wen Lu, "High-Speed Driving and Compact High- Speed Low-power Rail-to-Rail Class-B Buffer Amplifier for Small- and Large-size LCD Applications," accepted by *IEEE Journal of Solid-State Circuit.*

[26]. Ming-Chan Weng and Jiin-Chuan Wu, "A Compact Low- Power Rail-to-Rail Class-B Buffer for LCD Column Driver," *IEICE Trans. Electron.,* Vol. **E85-C**, No. 8 August, pp. 1659- 1663, 2002.

[27]. Pang-Cheng Yu and Jiin-Chuan Wu, "A Class-B Output Buffer for Flat-Panel-Display Column Driver," *IEEE Journal of Solid-State Circuits,* Vol. **34**, No.1, Jan. pp. 116-119, 1999.

[28]. Tetsuro Itaku, Hironori Minamizaki, Tetsuya Satio, and Tadashi Kuroda, "A 402-Output TFT-LCD Driver IC With Power Control Based on the Number of Colors Selected," *IEEE Journal of Solid-State Circuits,* Vol. **38**, No.3*, March*, pp. 503-510, 2003.

[29]. TFT-LCD source drivers NT39360, NT3982, and NT3994. Novatek. [Online]. Available: http://www.novatek.com.tw/.